AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

19. (previously presented): An information processing apparatus comprising:

a first computer module which includes a first controller and a second computer module which includes a second controller, wherein:

said first computer module includes a first processor, a first main-memory and a first sub-memory;

said second computer module includes a second processor, a second main-memory and a second sub-memory;

said first processor and said second processor operate substantially simultaneously and are substantially synchronized with each other;

said first controller writes data to said first main-memory and said second sub-memory according to a first write request of said first processor, and at the substantially same time, said second controller writes data to said second main-memory and said first sub-memory according to a second write request of said second processor;

wherein said first and second write requests are associated with the same data.

20. (previously presented): The information processing apparatus as claimed in claim 19, wherein said first controller controls so that while said first processor and said second processor are synchronized, read access from said first processor is carried out as against said first main-memory and write access from said first processor is carried out as against said first

main-memory and said second sub-memory and write access from said second processor is carried out as against said first sub-memory , and said first controller controls so that, when said first processor fails to be in synchronism with said second processor, read access from said first processor is carried out as against said first sub-memory and write access from said first processor is carried out as against said first main-memory, said first sub-memory and said second sub-memory.

21. (previously presented): The information processing apparatus as claimed in claim 20, wherein said first controller copies the contents of said first sub-memory to said first main-memory when said first processor fails to be in synchronism with said second processor.

22. (previously presented): The information processing apparatus as claimed in claim 21, wherein said first controller copies the contents of said first sub-memory to said first main-memory by means of a direct memory access circuit.

23. (previously presented): The information processing apparatus as claimed in claim 21, wherein said first processor recovers said synchronism with said second processor when said copy is completed for all memory areas of said first sub-memory.

24. (previously presented): The information processing apparatus as claimed in claim 22, wherein said first processor recovers said synchronism with said second processor when the copying is completed for all memory areas of said first sub-memory.

25. (currently amended): The information processing apparatus as claimed in claim 19, wherein said first and second controllers are connected as a ring for three or more otheranother computer modules.

26. (currently amended): The information processing apparatus as claimed in claim 20, wherein said first and second controllers arc connected as a ring for three or more otheranother computer modules.

27. (currently amended): The information processing apparatus as claimed in claim 21, wherein said first and second controllers are connected as a ring for three or more otheranother computer modules.

28. (currently amended): The information processing apparatus as claimed in claim 22, wherein said first and second controllers are connected as a ring for three or more otheranother computer modules.

29. (currently amended): The information processing apparatus as claimed in claim 23, wherein said first and second controllers are connected as a ring for three or more otheranother computer modules.

30. (currently amended): The information processing apparatus as claimed in claim 24, wherein said first and second controllers are connected as a ring for three or more otheranother computer modules.

31. (previously presented): The information processing apparatus as claimed in claim 19, wherein said first and second computer modules are on lockstep fault tolerant computer system.

32. (previously presented): The information processing apparatus as claimed in claim 20, wherein said first and second computer modules are on lockstep fault tolerant computer system.

33. (previously presented): The information processing apparatus as claimed in claim 21, wherein said first and second computer modules are on lockstep fault tolerant computer system.

34. (previously presented): The information processing apparatus as claimed in claim 22, wherein said first and second computer modules are on lockstep fault tolerant computer system.

35. (previously presented): The information processing apparatus as claimed in claim 24, wherein said first and second computer modules are on lockstep fault tolerant computer system.

36. (previously presented): The information processing apparatus as claimed in claim 30, wherein said first and second computer modules are on lockstep fault tolerant computer system.

37. (canceled).